

## QUALIFICATION FILE-Standalone NOS

### Fundamentals of Etching Techniques

- ☐ Horizontal/Generic ☐ Vertical/Specialization
- ☐ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA
- ☐ General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☐ OEM

NCrF/NSQF Level: 4.5

Submitted By:

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**Section 1: Basic Details**

1.	<b>NOS-Qualification Name</b>	<b>Fundamentals of Etching Techniques</b>																
2.	<b>Sector</b>	<b>Electronics</b>																
3.	<b>Type of Qualification</b> <input checked="" type="checkbox"/> New <input type="checkbox"/> Revised	<b>NQR Code &amp; version of the existing /previous qualification:</b> NA	<b>Qualification Name of the existing/previous version:</b> NA															
4.	<b>National Qualification Register (NQR) Code &amp; Version</b>	<b>NG-4.5-EH-03730-2025-V1-NIELIT</b>	<b>5. NCrF/NSQF Level:</b> 4.5															
6.	<b>Brief Description of the Standalone NOS</b>	This Standalone NOS provides foundational knowledge and practical skills in semiconductor manufacturing. It covers key processes like oxidation, etching (isotropic, anisotropic, and plasma-based), and advanced techniques such as ion-enhanced and high-density plasma etching. Participants will gain hands-on experience in process characterization, optimization, and integration, culminating in a final project. This course is ideal for those seeking expertise in microfabrication processes.																
7.	<b>Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee</b>	<b>a. Entry Qualification &amp; Relevant Experience:</b> <table border="1"> <thead> <tr> <th>S. No.</th> <th>Academic/Skill Qualification (with Specialization - if applicable)</th> <th>Required Experience (with Specialization - if applicable)</th> </tr> </thead> <tbody> <tr> <td>1.</td> <td>3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/ allied branches after class 10th</td> <td>NA</td> </tr> <tr> <td>2</td> <td>3rd year of 3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/ allied branches after class 10th</td> <td>NA</td> </tr> <tr> <td>3</td> <td>1<sup>st</sup> year of UG in Electronics Engineering/Physics/ allied fields</td> <td>NA</td> </tr> <tr> <td>4</td> <td>12th Pass</td> <td>1.5 year experience in ESDM Sector</td> </tr> </tbody> </table>		S. No.	Academic/Skill Qualification (with Specialization - if applicable)	Required Experience (with Specialization - if applicable)	1.	3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/ allied branches after class 10th	NA	2	3rd year of 3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/ allied branches after class 10th	NA	3	1 <sup>st</sup> year of UG in Electronics Engineering/Physics/ allied fields	NA	4	12th Pass	1.5 year experience in ESDM Sector
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1.	3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/ allied branches after class 10th	NA																
2	3rd year of 3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/ allied branches after class 10th	NA																
3	1 <sup>st</sup> year of UG in Electronics Engineering/Physics/ allied fields	NA																
4	12th Pass	1.5 year experience in ESDM Sector																

		5	10th pass plus 2-year NTC in relevant field of Electronics Sector		1.5-year experience in ESDM Sector													
8.	Credits Assigned to this NOS-Qualification, Subject to Assessment (as per National Credit Framework (NCrF))	1 Credit			9. Common Cost Norm Category (I/II/III) (wherever applicable): Category-I													
10.	Any Licensing Requirements for Undertaking Training on This Qualification (wherever applicable)	NA																
11.	Training Duration by Modes of Training Delivery (Specify Total Duration as per selected training delivery modes and as per requirement of the qualification)	<input checked="" type="checkbox"/> Offline <input type="checkbox"/> Online <input type="checkbox"/> Blended																
		Training Delivery Modes		Theory (Hours)	Practical (Hours)	Total (Hours)												
		Classroom (offline)		12	18	30												
12.	Assessment Criteria	<table><tr><td>Theory (Marks)</td><td>Practical (Marks)</td><td>Project (Marks)</td><td>Viva (Marks)</td><td>Total (Marks)</td><td>Passing %age</td></tr><tr><td>100</td><td>60</td><td>20</td><td>20</td><td>200</td><td>50</td></tr></table> <p>The centralized online assessment is conducted by the Examination Wing, NIELIT Headquarters.</p> <p>*Assessment strategy shall be as per NIELIT Norms prevailing at times.</p>					Theory (Marks)	Practical (Marks)	Project (Marks)	Viva (Marks)	Total (Marks)	Passing %age	100	60	20	20	200	50
Theory (Marks)	Practical (Marks)	Project (Marks)	Viva (Marks)	Total (Marks)	Passing %age													
100	60	20	20	200	50													
13.	Is the NOS Amenable to Persons with Disability	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No Leprosy Cured Person, Dwarfism, Thalassemia, Hemophilia, Hearing Impairment (Hard of Hearing), Acid Attack Victims.																
14.	Progression Path After Attaining the Qualification, wherever applicable (Please show Professional and Academic progression)	MEMS Backend Fabrication Engineer -> Semiconductor Fabrication Engineer																
15.	How participation of women will be encouraged?	Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women's participation under other schemes launched by the Government from time to time.																

16.	<b>Other Indian languages in which the Qualification &amp; Model Curriculum are being submitted</b>	Qualification file is available in English and Hindi languages.	
17.	<b>Is similar NOS available on NQR-if yes, justification for this qualification</b>	<input type="checkbox"/> Yes <input checked="" type="checkbox"/> No <b>URLs of similar Qualifications:</b>	
18.	<b>Name and Contact Details Submitting / Awarding Body SPOC</b> <i>(In case of CS or MS, provide details of both Lead AB &amp; Supporting ABs)</i>	<b>Name:</b> Sh. Ashwin Pawar <b>Email:</b> ashwin.pawar@nielit.gov.in <b>Contact No.:</b> 9425361315 <b>Website:</b> https://www.nielit.gov.in  <b>Name:</b> Sh. Saket Saurabh <b>Email:</b> srv.saket@nielit.gov.in <b>Contact No.:</b> 011-25308300 <b>Website:</b> https://www.nielit.gov.in	
19.	<b>Final Approval Date by NSQC:18.02.2025</b>	<b>20. Validity Duration: 3 Years</b>	<b>21. Next Review Date: 18.02.2028</b>

### Section 2: Training Related

1.	<b>Trainer's Qualification and experience in the relevant sector (in years) (as per NCVET guidelines)</b>	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control and allied branches with 2 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design. Or M.Sc. in Physics/Electronics/Material Science and allied branches; with 2 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design.
2.	<b>Master Trainer's Qualification and experience in the relevant sector (in years) (as per NCVET guidelines)</b>	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control and allied branches with 3 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design. Or M.Sc. in Physics/Electronics/Material Science and allied branches; with 3 years of relevant

		experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design.
3.	<b>Tools and Equipment Required for Training</b>	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No Available at Annexure-II
4.	<b>In Case of Revised Qualification, Details of Any Upskilling Required for Trainer</b>	NA

### Section 3: Assessment Related

1.	<b>Assessor's Qualification and experience in relevant sector (in years) (as per NCVET guidelines)</b>	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control and allied branches with 3 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design. Or M.Sc. in Physics/Electronics/Material Science and allied branches 3 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design.
2.	<b>Proctor's Qualification and experience in relevant sector (in years) (as per NCVET guidelines)</b>	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online, and the paper comprise of MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I- card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds.
3.	<b>Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years) (as per NCVET guidelines)</b>	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech.
4.	<b>Assessment Mode (Specify the assessment mode)</b>	Centralized online examination will be conducted
5.	<b>Tools and Equipment Required for Assessment</b>	<input checked="" type="checkbox"/> Same as for training <input type="checkbox"/> Yes <input type="checkbox"/> No (details to be provided in Annexure-if it is different for Assessment)

**Section 4: Evidence of the Need for the Standalone NOS**

1.	Government /Industry initiatives/ requirement (Yes/No): Yes
2.	Number of Industry validation provided: The course has been developed in collaboration with TATA Electronics to support the development of skilled manpower for the upcoming semiconductor industry.
3.	Estimated number of people to be trained: 500
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): No  NIELIT is recognized as an Adjudicating Body (AB) and Assessment Body (AA) under the Government category. NIELIT is the Human Resource Development (HRD) arm of MeitY, therefore, the Line Ministry Concurrence is not required.

**Section 5: Annexure & Supporting Documents Check List**

Specify Annexure Name / Supporting document file name

1.	<b>Annexure:</b> NCrf/NSQF level justification based on NCrf level/NSQF descriptors ( <i>Mandatory</i> )	Available at Annexure-I: Evidence of Level
2.	<b>Annexure:</b> List of tools and equipment relevant for qualification ( <i>Mandatory, except in case of online course</i> )	Available at Annexure-II: Tools and Equipment
3.	<b>Annexure:</b> Industry Validation	Available at Annexure-III: Industry Validation
4.	<b>Annexure: Training Details</b>	Available at Annexure-IV: Training Details
5.	<b>Annexure:</b> Blended Learning ( <i>Mandatory, in case selected Mode of delivery is "Blended Learning"</i> )	Available at Annexure-V: Blended Learning
6.	<b>Annexure/Supporting Document:</b> Standalone NOS- Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	Available at Annexure-VI: Standalone NOS- Performance Criteria details
7.	<b>Annexure:</b> Detailed Assessment Criteria ( <i>Mandatory</i> )	Available at Annexure-VII: Assessment Criteria
8.	<b>Annexure:</b> Assessment Strategy ( <i>Mandatory</i> )	Available at Annexure-VIII: Assessment Strategy

9.	<b>Annexure:</b> Acronym and Glossary ( <i>Optional</i> )	Available at Annexure-IX: Acronym and Glossary
10.	<b>Supporting Document:</b> Model Curriculum ( <i>Mandatory – Public view</i> )	Available at Annexure-A: Model Curriculum

**Annexure I: Evidence of Level**

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
<b>Professional Theoretical Knowledge/Process</b>	<ul style="list-style-type: none"> <li>Understanding of Etching and Deposition Techniques in Semiconductor Manufacturing and to Silicon Dioxide Structure and Its Role in Semiconductors</li> </ul>	<ul style="list-style-type: none"> <li>Provides foundational Etching and Deposition Techniques in Semiconductor Manufacturing</li> </ul>	4.5
<b>Professional and Technical Skills/ Expertise/ Professional Knowledge</b>	<ul style="list-style-type: none"> <li>Proficiency in Basics of Etching- Isotropic and Anisotropic Etching and Chemical Mechanisms in Etching Processes</li> </ul>	<ul style="list-style-type: none"> <li>Equips learners with technical skills to analyze and enhance semiconductor designs and manufacturing.</li> </ul>	4.5
<b>Employment Readiness &amp; Entrepreneurship Skills &amp; Mind-set/Professional Skill</b>	<ul style="list-style-type: none"> <li>Prepared for roles like Semiconductor Deposition Engineer or Layout Analyst; skilled in problem-solving, teamwork, and technical communication.</li> </ul>	<ul style="list-style-type: none"> <li>Aligns job readiness and entrepreneurial mindset with industry requirements and collaborative practices.</li> </ul>	4.5
<b>Broad Learning Outcomes/Core Skill and Responsibility</b>	<ul style="list-style-type: none"> <li>Accountability for resolving manufacturability issues, optimizing designs, and ensuring yield and quality through collaboration and technical expertise.</li> </ul>	<ul style="list-style-type: none"> <li>Prepares learners to take ownership of critical tasks in design and manufacturing with measurable impact.</li> </ul>	4.5

**Annexure II: Tools and Equipment (Lab Set-Up)****List of Tools and Equipment**

Sl. No	Description	Qty.	Specifications
1	Classroom	1	30 Sq. m
2	Student Chair	30	-
3	Student Table	30	-
4	LCD Projector	1	-
5	Trainer Chair & Table	1	-
6	Pin up Board	1	-
7	White Board	1	-
8	Desktop Computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent Memory: 16GB RAM, Internal Storage: 500GB
9	Desk jet printer	1	A4

**Tools and Equipment:**

- Etching Tools
- Deposition Tools
- Measurement and Characterization Tools
- Process Control Tools
- Chemical Handling and Safety Tools
- General Equipment
- Consumables

**Annexure III: Industry Validations Summary**

The course has been developed in collaboration with TATA Electronics to support the development of skilled manpower for the upcoming semiconductor industry.

**Annexure IV: Training & Employment Details****Training Projections:**

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2025-26	100	50	10
2026-27	200	70	15
2027-28	200	70	15

*Data to be provided year-wise for next 3 years.*

**Annexure V: Blended Learning**

**Blended Learning Estimated Ratio & Recommended Tools: NA**

**Annexure VI: Performance Criteria details****1. Description:**

The "Fundamentals of Etching Techniques" course equips learners with foundational knowledge and hands-on skills in semiconductor manufacturing processes. It covers oxidation, etching, plasma-based techniques, and process integration. Participants will develop the expertise to analyze, optimize, and implement fabrication techniques effectively.

**2. Scope:**

- Develop theoretical and practical knowledge of etching and deposition processes, including oxidation, isotropic/anisotropic etching, and plasma-based techniques.
- Gain expertise in operating fabrication equipment, measuring layer properties, and analyzing process outcomes for quality and uniformity.  
Learn to integrate and optimize etching and deposition processes for semiconductor manufacturing, ensuring precision and efficiency in microfabrication tasks.

### 3. Elements and Performance Criteria

To be competent, the user/individual on the job must be able to:

Elements	Performance Criteria
<b>Introduction to Etching and Deposition Techniques</b>	<b>PC1:</b> Demonstrate understanding of the principles of etching and deposition and their significance in semiconductor manufacturing <b>PC2:</b> Explain the role of silicon dioxide in semiconductors, including its structural and functional importance.
<b>Oxidation Processes</b>	<b>PC3:</b> Distinguish between dry and wet oxidation processes, describing their mechanisms, applications, and limitations. <b>PC4:</b> Conduct and analyze oxidation processes, evaluating rates, oxide quality, and suitability for semiconductor applications.
<b>Basics of Etching</b>	<b>PC5:</b> Explain the fundamentals of isotropic and anisotropic etching and their relevance to semiconductor fabrication. <b>PC6:</b> Perform etching techniques, measure etch profiles, and evaluate results for process accuracy and effectiveness.
<b>Plasma-Based Dry Etching</b>	<b>PC7:</b> Demonstrate knowledge of plasma etching techniques, including the role of plasma in achieving precision etching. <b>PC8:</b> Operate plasma etching equipment and optimize parameters to achieve desired etching results and uniformity.
<b>Advanced Etching Techniques</b>	<b>PC9:</b> Explain principles of ion-enhanced etching and high-density plasma (HDP) etching, including their benefits and applications. <b>PC10:</b> Perform advanced etching processes and evaluate quality metrics, such as uniformity, accuracy, and material compatibility.
<b>Process Integration and Final Project</b>	<b>PC11:</b> Demonstrate integration of etching and deposition processes, focusing on optimization and control for improved outcomes. <b>PC12:</b> Design, implement, and evaluate a complete etching and deposition process as part of a final project, showcasing practical expertise and theoretical understanding.

#### 4. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

**KU1:** Understand the principles and applications of etching and deposition techniques in semiconductor manufacturing, including their impact on device performance and process efficiency.

**KU2:** Gain knowledge of material selection, process compatibility, and how they affect manufacturability, product reliability, and production efficiency.

**KU3:** Develop familiarity with tools and techniques for characterizing thin films, measuring etch profiles, and analyzing process outcomes in laboratory settings.

#### 5. Generic Skills (GS):

The user/individual on the job needs to know how to:

**GS1:** Identify and troubleshoot challenges in etching and deposition processes, applying critical thinking to optimize fabrication techniques for improved yield, uniformity, and reliability.

**GS2:** Communicate technical findings effectively, collaborate with cross-functional teams (e.g., process engineers, designers, and quality analysts), and present process optimizations clearly and concisely.

**GS3:** Leverage analytical and decision-making skills to evaluate process outcomes, refine parameters, and achieve desired fabrication goals.

**Annexure VII: Assessment Criteria**

Detailed assessment criteria for each NOS/Module are as follows:

Elements	Assessment Criteria for Performance Criteria/Learning Outcomes	Theory Marks	Practical Marks	Project Marks	Viva Marks
<b>Introduction to Etching and Deposition Techniques</b>	<b>PC1:</b> Demonstrate understanding of the principles of etching and deposition and their significance in semiconductor manufacturing <b>PC2:</b> Explain the role of silicon dioxide in semiconductors, including its structural and functional importance.	<b>16</b>	<b>12</b>	-	-
<b>Oxidation Processes</b>	<b>PC3:</b> Distinguish between dry and wet oxidation processes, describing their mechanisms, applications, and limitations. <b>PC4:</b> Conduct and analyze oxidation processes, evaluating rates, oxide quality, and suitability for semiconductor applications.	<b>16</b>	<b>12</b>	-	-
<b>Basics of Etching</b>	<b>PC5:</b> Explain the fundamentals of isotropic and anisotropic etching and their relevance to semiconductor fabrication. <b>PC6:</b> Perform etching techniques, measure etch profiles, and evaluate results for process accuracy and effectiveness.	<b>17</b>	<b>12</b>	-	-
<b>Plasma-Based Dry Etching</b>	<b>PC7:</b> Demonstrate knowledge of plasma etching techniques, including the role of plasma in achieving precision etching. <b>PC8:</b> Operate plasma etching equipment and optimize parameters to achieve desired etching results and uniformity.	<b>17</b>	<b>12</b>	-	-
<b>Advanced Etching Techniques</b>	<b>PC9:</b> Explain principles of ion-enhanced etching and high-density plasma (HDP) etching, including their benefits and applications. <b>PC10:</b> Perform advanced etching processes and evaluate quality metrics, such as uniformity, accuracy, and material compatibility.	<b>17</b>	<b>12</b>	-	-
<b>Process Integration and Final Project</b>	<b>PC11:</b> Demonstrate integration of etching and deposition processes, focusing on optimization and control for improved outcomes. <b>PC12:</b> Design, implement, and evaluate a complete etching and deposition process as part of a final project, showcasing practical expertise and theoretical understanding.	<b>17</b>	-	<b>20</b>	-
<b>Viva</b>	Including all elements	-	-	-	<b>20</b>
<b>GRAND TOTAL</b>		<b>100</b>	<b>60</b>	<b>20</b>	<b>20</b>

### **Annexure VIII: Assessment Strategy**

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.

The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. Competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

#### **About Examination Pattern:**

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.
2. The assessor assigns roll number.
3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ
4. Pass percentage would be 50% marks.
5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

**Annexure-IX: Acronym and Glossary**

## Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

## Glossary

Term	Description
<b>National Occupational Standards (NOS)</b>	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
<b>Qualification</b>	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
<b>Qualification File</b>	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
<b>Sector</b>	A grouping of professional activities on the basis of their main economic function, product, service or technology.