Annexure - I

Course Content
For
PG- Diploma VLSI Design

Course Modules:

Sr. No.	Module Name	No of Theory Hours	No of Lab Hours	No of Hours
1	Advanced Digital Design	24	-	24
2	System Architecture	36	-	36
3	Programming Fundamentals	30	40	70
4	High Level Design Methodology	30	80	110
5	HDL Simulation and Synthesis	32	78	110
6	Verilog (In accordance with IEEE 1364-2005 & 2009)	30	90	120
7	ASIC Design Issues	10	30	40
8	CMOS VLSI Design	20	-	20
9	Verification using System Verilog	40	50	90
10	Linux shell scripting & Perl	22	38	60
11	Effective Communication	50	-	50
12	Aptitude & English	50	-	50
13	Project	-	120	120
	Total			**900**

Course Contents:

1. **Advanced Digital Design** **(24 Theory hrs)**
   - Combinatorial Logic Design
   - Sequential Logic Design : State machines
   - Advanced Design Issues: metastability, noise margins, power, fan-out, design rules, skew, timing considerations.
   - Asynchronous State Machine- cycle stealing using latch in synchronous circuits, Interfacing Asynchronous data flow, Asynchronous FIFO design

2. **System Architectures** **(36 Theory hrs)**
   - System Building Blocks
     - Computer Architecture
     - Memory Architectures
     - Introduction to a system bus (PCI- Express)
     - Introduction to peripheral bus (USB)
     - Introduction to a LAN (Ethernet)
   - FPGA Architecture
     - Architecture study of some popular FPGA families
     - Detailed study of a Xilinx high end FPGA family

- Architecture of Microcontrollers in FPGA(ARM)
- The backend tools
- Integrating non-HDL modules : Building macros
- Introduction to SOC

3. Programming Fundamental (30Theory + 40lab)

- Introduction to C
- Arrays
- Functions
- Strings
- Structures & unions
- Introduction to C++
- Classes & Objects
- Inheritance
- Class and Function Templates,
- Exception Handling,
- Namespaces

4. VHDL (In accordance with standard IEEE 1076-2008) (30Theory + 80 Lab)

- Introduction to HDL
- VHDL Flow
- Language constructs
- Concurrent constructs
- Sequential Constructs
- Subprogram
- Packaging
- Timing Issues

5. HDL Simulation and Synthesis (32Theory + 78 Lab)

- The concept of Simulation
- HDL Simulation and Modeling
- The Synthesis Concept
- Synthesis of high level constructs
- Timing Analysis of Logic circuits
- Combinatorial Logic Synthesis
- State machine synthesis
- Efficient coding styles
- Hierarchical and flat designs
- Constraining designs
- Partitioning for synthesis
- Pipelining
- Resource sharing
- Optimizing arithmetic expressions
- Design reuse
- The Simulation and Synthesis Tools
- FPGA synthesis and implementation

6. **Verilog (In accordance with IEEE 1364-2005 and 2009) (30Theory + 90 lab)**
    - Data types
    - Modeling concepts,
    - Task and Functions
    - Specify block and Timing checks
    - Verification and Writing test benches

7. **ASIC Design (10 Theory + 30 Lab)**
    - Introduction of Full custom and semi custom ASIC Design Flow and Flow Diagram
    - Specifications and Schematic cell Design.
    - Spice simulation Analysis of analog and digital circuits, circuit elements, AC and DC analysis.
    - Transfer Characteristics, Transient responses, Noise analysis of current and voltage.
    - Design Rule, Micron Rules, Lambda rules of the design and design rule check.
    - Fabrication methods of circuit elements, Layout design of different cells like Diff. Library cell designing, NAND, NOR, NOT, X-OR etc.
    - Circuit Extraction, Electrical rule check, LVS, Post-layout Simulation and Parasitic extraction.
    - Different design Issues like Antenna effect, Electro migration effect, Body effect, Inductive and capacitive cross talk and Drain punch through, etc.
    - Design format, Timing analysis, Back notation and Post layout simulation
    - DFT Guideline, Test Pattern and BIST
    - ASIC design implementation

8. **CMOS VLSI Design (20 Theory)**
    - Introduction of MOS device
    - N- Mos , P-Mos and CMOS
    - Structure of MOS cells
    - Threshold Voltage,
    - CMOS Inverter Characteristics, Device sizing,
    - Rationed and non rationed logic.
    - CMOS combinational logic design, Design of Basic gates, transmission gates and Design of complex logic circuit.
    - Latch Up effect , Body Effect,
    - Channel Length Modulation,
    - CMOS as a switch,
    - Noise Margin,
    - Capacitance Estimation
    - Rise and fall times
    - Power dissipation and Design of complex circuit fabrication steps.

9. **Verification using SystemVerilog (40 Theory + 50 lab)**
    - Introduction to Verification
    - Types of verification

- Code coverage
- Introduction to SystemVerilog
- Introduction to task & functions in SystemVerilog
- OOPs Terminology
- Implementation of OOPs Concepts in SystemVerilog
- Randomization
- Case Studies
- Assertions property
- Assertions Time
- Functional Coverage
- Overview of UVM Verification Methodology

10. Linux Shell Scripting& Perl **(22 Theory + 38 lab)**

- Linux Commands
- Linux File System
- Vi editor,
- The Shell
- Shell Programming
- Perl
- Basic of tcl/tk scripting

11. Project **120 Hrs**