Annexure - I

Certified VLSI Design Engineer

(Model Curriculum)

Annexure 1
Detailed Syllabus of Course

S. No	Module Title	Topics	Duration (Hours)		Learning Outcome
			Theory	Lab	
1.	**INTRODUCTION TO DIGITAL ELECTRONICS**	• Introduction to Number Systems, Logic Gates • Understanding Combinational Logic Circuit Designing -Adder, Subtractor, MUX, DEMUX, Encoder and Decoder etc. • Understanding Sequential Logic Circuit Designing- Latches, Flipflops, Counter, Register etc. • Introduction to Finite state machine (FSM) • Moore's Machine and Mealy's Machine.	20	15	After going through this module student will Understand the basics of digital electronics
2.	**INTRODUCTION TO VLSI**	• Need, Scope, Use and History of VLSI • Introduction to Chip Design Process • Description of Hardware Description Languages • Applications of VLSI • VLSI Design Flow • Moore's Laws • VLSI Design Flow and Y-Chart • Front-Back End VLSI Design	20	15	Student would be able to understand need, history and application of VLSI Technology .
3.	**VERILOG HDL**	• Overview of Digital Design with Verilog HDL Evolution of CAD • Emergence of HDLs, typical HDL-based design flow • Why Verilog HDL, trends in HDLs. • Hierarchical Modeling Concepts • Top-down and bottom-up design methodology	20	30	Students Will be able to know how to do circuit designing using HDL language

		• Differences between modules and module instances • Parts of a simulation, design block, stimulus block • Basic Concepts Lexical conventions • Data types, system tasks, compiler directives • Modules and Ports Module definition • Port declaration, connecting ports • Hierarchical name referencing			
4.	**MODELING TECHNIQUES**	• Gate-Level Modeling • Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise • Fall and tum-off delays, min, max, and typical delays. Dataflow Modeling • Continuous assignments • Delay specification, expressions, operators, operands, operator types • Behavioural Modeling Structured procedures • Initial and always, blocking and nonblocking statements • Delay control, Event control • Conditional statements, multiway branching loops, sequential and parallel blocks • Tasks and Functions • Differences between tasks and functions • Declaration, invocation • Useful Modeling Techniques • Procedural continuous assignments • Overriding parameters	30	40	Students are introduced to the knowledge of various types of Modelling Techniques used in VLSI

		• Conditional compilation and execution • Useful system tasks.			
5.	**FPGA ARCHITECTURE AND PROTOTYPING**	• Introduction to FPGA, Architecture • Internal resource and Design Essentials • FPGA Input/output Blocks (IOBs), Special FPGA functions • Logic Synthesis, FPGA Programming with Verilog basics, Tool Training • Different Voltage Requirement's for FPGA • Different External memory devices architecture • IO Planning, Report analysis for Timing, Area and Power • CPLD, FPGA working, References, Design flow, Design tricks • H/W components on FPGA board and their working • Designing basic FPGA examples (Adder, Subtractor, Counter etc.)	20	30	Students learn the basics of FPGA Technology and its applications They would able to create various circuits using FPGA technology
6.	**INTRODUCTION TO THE MOS TECHNOLOGY**	• Introduction to IC technology MOS, PMOS, NMOS, CMOS & BiCMOS Technologies • Basic Electrical Properties of MOS and BiCMOS Circuits • IDS - VDS relationships • MOS transistor Threshold Voltage • Figure of merit, Transconductance • Pass transistor	20	30	Students will able to understand basics of MOSFET technology, their characteristics, and fabrication Process.

		• NMOS Inverter, Various pull ups • CMOS Inverter analysis and design • Bi-CMOS Inverters • Fabrication Process Flow • Transmission gates etc • Device sizing, timing parameters • Estimation of layout resistance & capacitance			
7.	**VLSI CIRCUIT DESIGN PROCESSES**	• VLSI Design Flow • MOS Layers • Stick Diagrams, Design Rules and Layout • Lambda(λ)-based design rules for wires, contacts and Transistors • Layout Diagrams for NMOS and CMOS Inverters and Gates • Scaling of MOS circuits, Limitations of Scaling. • Introduction to simulation tools • Place and Route Extraction, LVS • Netlist to GDS-II flow • Device Generator Libraries • SPICE Modelling, SPICE Tutorials and Commands • Sources and Passive Components • Inverter Transient	30	40	Students will able to understand VLSI circuit designing Process, Design rules, Modelling of devices etc
8.	**DESIGN VERIFICATION UVM, OVM AND AVM METHODOLOGY**	• Introduction UVM, UVM Object • UVM test Bench etc. • Introduction OVM, OVM Reporting • OVM Transaction • OVM Configuration etc.	20	40	Students will able to understand various Design verification techniques like UVM, OVM and AVM.

		• Need for File Inter Change • GDS2 Stream, Caltech Intermediate Format (CIF) • Library Exchange Format (LEF) • Design Exchange Format (DEF), Standard Delay Format (SDF), DSPF • SPEF, Advance Library Format (ALE), Waves Waveform and Vector Exchange • Specification, Physical Design Exchange Format, Open Access			
		Sub-total	180	240	
9.	**Employability Skills**	• Introduction to Employability Skills • Career Development & Goal Setting • Becoming a Professional in the 21st Century • Basic English Skills • Communication Skills • Financial and Legal Literacy • Entrepreneurship • Diversity & Inclusion • Constitutional values - Citizenship • Essential Digital Skill	30		
10.	**OJT**		30		
		Total	**480**		

Recommended Hardware:	• Desktop PC's with 16GB RAM, 1TB HDD, or Higher • FPGA Development platform Kit • VLSI Trainer Kit

Recommended Software:	• CADENCE TOOL • XILINX TOOL • SILVACO ATLAS TCAD • ORCAD
Text Books:	• Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP. • Douglas A.Pucknell& Kamran Eshraghian, Basic VLSI Design, PHI Publication. • J.Rabaey, Digital Integrated circuits, PHI Publication.
Reference Books:	• Sung-mo Kang and Yusuf Leblebici, CMOS Digital ICs, TMH Publication • Verilog HDL , A guide to Digital Design and Synthesis Samir Palnitkar SunSoft Press Publications

Section 2

LIST OF EQUIPMENT (For a batch of 10 students)

Description		**Qty**	**Specifications**
1	Classroom	1	30 Sq M
2	Student Chairs	10	
3	Student Tables	10	
4	Computer with latest configuration & Internet	5	
5	Laptop with latest configuration	1	
5	LCD Projector	1	
6	Trainer Chair & Table	1	
7	White Board for teaching	1	
	Computer Lab		
1	Desktop computer with latest configurations & accessories	5	Installed with VSLI Design Softwares
2	Laser jet printer	1	

Section 3

TRAINER PROFILE

Level: 5

Batch Size: 10 students

No of Trainers: 1

No of demonstrators: 1

Education Qualification	Engineer / Electronics/Electrical/Instrumentation Engineering
Experience	• Minimum 2 years' experience in a reputed VLSI Design Company, training institute or organization as a trainer
Technical Skills	• Hands on Knowledge of VLSI Design Softwares • Good understanding of Basic of Electronics and VLSI
Other Skills	• Should be able to communicate well in English • Knowledge of working on computers • Should be able to prepare lesson plan, deliver the courses through the specified media as per schedule • Should be able to aspire the trainees &evaluate and assess the trainees • Should be able to monitor progress and give feedback to trainees • Should be able to maintain MIS related to training

Section 4

LIST OF OTHER SOFTWARE (For a batch of 10 students)

1. Primary requirement	
Operating system	For all computers
Web browser	
Antivirus	
Internet connectivity	

From the following software one from each group need to be installed in minimum 10 work stations. Original licenses need to be obtained wherever necessary. Open-source software's are allowed.

2. Software for Documentation, Calculation & Presentation	
Proprietary Software	MS Office
Open Software	Libre Office

3. Software for VLSI DESIGN	
Proprietary Software	● CADENCE TOOL ● XILINX TOOL ● SILVACO ATLAS TCAD ● ORCAD