NSQF QUALIFICATION FILE
Approved in 22nd NSQC – NCVET, Dated: 25th August, 2022

NCVET Code
2022/EHW/NIELIT/06345

CONTACT DETAILS OF THE BODY SUBMITTING THE QUALIFICATION FILE

Name and address of submitting body:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY
NIELIT Bhawan,
Plot No. 3, PSP Pocket, Sector-8,
Dwarka, New Delhi-110077

Name and contact details of individual dealing with the submission

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List of documents submitted in support of the Qualifications File

Annexure 1: Model Curriculum
Annexure 2: Evidence of Need

SUMMARY

1	**Qualification Title**	Certified VLSI Design Engineer
2	**Qualification Code**	
3	**NCO Code and Occupation**	2152.050: Design Engineer
4	**Nature and Purpose of Qualification**	Nature: ● Course will help in Employment in the area of VLSI Design Purpose: ● To Provide Employment in Electronic Circuit Designing, Testing Industries. ● To upgrade the skills of incumbent working in field of Analog, Digital & Mixed VLSI Integrated circuits, ● Entrepreneurship Development.
5	**Body/bodies which will award the qualification.**	National Institute of Electronics and Information Technology (NIELIT) NIELIT Bhawan, Plot No. 3, PSP Pocket, Sector-8, Dwarka, New Delhi-110077
6	**Body which will accredit providers to offer the qualification.**	NIELIT
7	**Whether accreditation/affiliation norms are already in place or not , if applicable (if yes, attach a copy)**	Yes, Available at www.nielit.gov.in
8	**Occupation(s) to which the qualification gives access**	● VLSI Design Engineer ● Circuit Test Engineer ● Design and Verification Engineer ● VLSI Programmer

9	**Job description of the occupation**	• Designing of VLSI circuits • Designing of Embedded Systems • Fault & Error identification in Digital Circuits
10	**Licensing requirement**	NA
11	**Statutory and Regulatory requirement of the relevant sector (documentary evidence to be provided)**	NA
12	**Level of the qualification in the NSQF.**	Level 5
13	**Anticipated volume of training/learning required to complete the qualification**	480 Theory: 180 Practical: 240 OJT: 30 ES: 30
14	**Indicative list of training tools required to deliver this qualification**	Available at Annexure-I
15	**Entry requirements / recommendations. And minimum age**	Graduation in relevant Field or 2 years diploma after class 12th with 1 years of Experience in the relevant field. or 3 years diploma after class 10th with 2 years of Experience in the relevant field.
16	**Progression from the qualification.**	**Academic:** This course is frequently updated in synchronization with the industry to provide the trainees in-depth knowledge and skills required by Embedded & VLSI markets around the globe. It provides comprehensive understanding about the fundamental principles, methodologies and industry practices.

		Professional: This uniquely hybrid course makes the successful participants readily employable in multiple roles available in broad spectrum of relevant industries like: (a) Circuit Layout Designing (b) Circuit Testing **Research and Development:** For people interested in entrepreneurships this would be an excellent launch pad. In addition, the course also serves as a concrete platform for people involved in application research, consultancy and high-end product development in both industry and academia.		
17	**Arrangements for the Recognition of Prior learning (RPL)**	The candidates who will undergo training shall only be assessed.		
18	**International comparability** **Where known (research evidence to be provided)**	NA		
19	**Date of planned review of qualification**	25/08/2025		
20	**Formal structure of the qualification** **Mandatory components**			
	Title of component and identification code/NOSs/Learning outcomes		**Estimated size (learning hours)**	**Level**
1	**INTRODUCTION TO DIGITAL ELECTRONICS** • Introduction to Number Systems, Logic Gates • Understanding Combinational Logic Circuit Designing -Adder, Subtractor, MUX, DEMUX, Encoder and Decoder etc.		35 Hours	Level 5

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	• Understanding Sequential Logic Circuit Designing-Latches, Flipflops, Counter, Register etc. • Introduction to Finite state machine (FSM) • Moore's Machine and Mealy's Machine.		
2	**INTRODUCTION TO VLSI** • Need, Scope, Use and History of VLSI • Introduction to Chip Design Process • Description of Hardware Description Languages • Applications of VLSI • VLSI Design Flow • Moore's Laws • VLSI Design Flow and Y-Chart • Front-Back End VLSI Design	35 Hours	Level 5
3	**VERILOG HDL** • Overview of Digital Design with Verilog HDL • Evolution of CAD • Emergence of HDLs, typical HDL-based design flow • Why Verilog HDL, trends in HDLs. • Hierarchical Modeling Concepts • Top-down and bottom-up design methodology • Differences between modules and module instances • Parts of a simulation, design block, stimulus block • Basic Concepts Lexical conventions • Data types, system tasks, compiler directives • Modules and Ports Module definition • Port declaration, connecting ports • Hierarchical name referencing	50 Hours	Level 5
4	**MODELING TECHNIQUES** • Gate-Level Modeling • Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise • Fall and tum-off delays, min, max, and typical delays. Dataflow Modeling • Continuous assignments • Delay specification, expressions, operators, operands, operator types • Behavioural Modeling Structured procedures • Initial and always, blocking and nonblocking statements • Delay control, Event control • Conditional statements, multiway branching loops, sequential and parallel blocks	70 Hours	Level 5

	• Tasks and Functions • Differences between tasks and functions • Declaration, invocation • Useful Modeling Techniques • Procedural continuous assignments • Overriding parameters • Conditional compilation and execution • Useful system tasks.		
5	**FPGA ARCHITECTURE AND PROTOTYPING** • Introduction to FPGA, Architecture • Internal resource and Design Essentials • FPGA Input/output Blocks (IOBs), Special FPGA functions • Logic Synthesis, FPGA Programming with Verilog basics, Tool Training • Different Voltage Requirement's for FPGA • Different External memory devices architecture • IO Planning, Report analysis for Timing, Area and Power • CPLD, FPGA working, References, Design flow, Design tricks • H/W components on FPGA board and their working • Designing basic FPGA examples (Adder, Subtractor, Counter etc.)	50 Hours	Level 5
6	**INTRODUCTION TO THE MOS TECHNOLOGY** • Introduction to IC technology MOS, PMOS, NMOS, CMOS & BiCMOS Technologies • Basic Electrical Properties of MOS and BiCMOS Circuits • IDS - VDS relationships • MOS transistor Threshold Voltage • Figure of merit, Transconductance • Pass transistor • NMOS Inverter, Various pull ups • CMOS Inverter analysis and design • Bi-CMOS Inverters • Fabrication Process Flow • Transmission gates etc • Device sizing, timing parameters • Estimation of layout resistance & capacitance	50 Hours	Level 5

7	**VLSI CIRCUIT DESIGN PROCESSES** ● VLSI Design Flow ● MOS Layers ● Stick Diagrams, Design Rules and Layout ● Lambda(λ)-based design rules for wires, contacts and Transistors ● Layout Diagrams for NMOS and CMOS Inverters and Gates ● Scaling of MOS circuits, Limitations of Scaling. ● Introduction to simulation tools ● Place and Route Extraction, LVS ● Netlist to GDS-II flow ● Device Generator Libraries ● SPICE Modelling, SPICE Tutorials and Commands ● Sources and Passive Components ● Inverter Transient	70 Hours	Level 5
8	**DESIGN VERIFICATION UVM, OVM AND AVM METHODOLOGY** ● Introduction UVM, UVM Object ● UVM test Bench etc. ● Introduction OVM, OVM Reporting ● OVM Transaction ● OVM Configuration etc. ● Need for File Inter Change ● GDS2 Stream, Caltech Intermediate Format (CIF) ● Library Exchange Format (LEF) ● Design Exchange Format (DEF), Standard Delay Format (SDF), DSPF ● SPEF, Advance Library Format (ALE), Waves Waveform and Vector Exchange ● Specification, Physical Design Exchange Format, Open Access	60 Hours	Level 5
	Sub-Total	420	

9	**Employability Skills** ● Introduction to Employability Skills ● Career Development & Goal Setting ● Becoming a Professional in the 21st Century ● Basic English Skills ● Communication Skills ● Financial and Legal Literacy ● Entrepreneurship ● Diversity & Inclusion ● Constitutional values - Citizenship ● Essential Digital Skill	30 Hours	
10	**On Job Training**	30 Hours	
	Total	**480 Hours**	

SECTION 1

ASSESSMENT

21	**Body/Bodies which will carry out assessment:** The Examination Section National Institute of Electronics and Information Technology NIELIT Bhawan, Plot No. 3, PSP Pocket, Sector-8, Dwarka, New Delhi-110077
22	**How will the assessment body be responsible for RPL assessment?** The candidates who will undergo training shall only be assessed.

23	**Describe the overall assessment strategy and specific arrangements which have been put in place to ensure that assessment is always valid, consistent and fair and show that these are in line with the requirements of the NSQF:** The emphasis is on theory as well as on practical & knowledge based on the performance criteria. Student is required to pass in all evaluations individually and marks will be allotted. The Following assessment methodologies are used. A. Written Assessment. B. Practical Assessment & class Performance. C. Viva-Voce. D. Project. The assessment results are backed by following evidences. 1. The assessor collects a copy of the attendance for the training done under the scheme. The attendance sheets are signed and stamped by the In-charge / Head of the Training Centre. 2. The assessor verifies the authenticity of the candidate by checking the photo ID card issued by the institute as well as any one Photo ID card issued by the Central/Government. The same is mentioned in the attendance sheet. 3. The assessor assigns roll number. 4. The assessor takes photograph of all the students along with the assessor standing in the middle and with the centre name/banner at the back as evidence.

ASSESSMENT EVIDENCE

Title of Unit/Component:

Outcomes to be assessed/NOSs to be assesed	Assessment criteria for the outcome	Total Mark
OUTCOME-1: After going through this module student will Understand the basics of digital electronics	• Introduction to Number Systems, Logic Gates • Understanding Combinational Logic Circuit • Encoder and Decoder etc. • Understanding Sequential Logic Circuit	**20**

OUTCOME-2: Student would be able to understand need, history and application of VLSI Technology .	• Need, Scope, Use and History of VLSI • Introduction to Chip Design Process • Description of Hardware Description Languages • Applications of VLSI • VLSI Design Flow • Moore's Laws • VLSI Design Flow and Y-Chart • Front-Back End VLSI Design .	**20**
OUTCOME-3: Students Will be able to know how to do circuit designing using HDL language	• Overview HDL • Verilog HDL, • Hierarchical Modelling Concepts • simulation, design block, stimulus block	**20**
OUTCOME-4: Students are introduced to modelling techniques	• Gate-Level Modeling • Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise • Continuous assignments • Delay specification, • Behavioural Modeling Structured procedures • Conditional statements, multiway branching loops, sequential and parallel blocks • Tasks and Functions	**20**
OUTCOME-5: Students learn the basics of FPGA Technology and its applications They would able to create various circuits using FPGA technology	• Introduction to FPGA, Architecture • FPGA Input/output Blocks (IOBs), Special FPGA functions • Logic Synthesis, FPGA Programming with Verilog basics, Tool Training • Different Voltage Requirement's for FPGA • Designing basic FPGA examples (Adder, Subtractor, Counter etc.)	**20**

OUTCOME-6: Students will able to understand basics of MOSFET technology, their characteristics, and fabrication Process.	• Introduction to IC technology MOS, PMOS, NMOS, CMOS & BiCMOS Technologies • Transmission gates etc • Device sizing, timing • parameters • Estimation of layout resistance & capacitance	**20**
OUTCOME-7: Students will able to understand VLSI circuit designing Process, Design rules, Modelling of devices etc	• VLSI Design Flow • MOS Layers • Stick Diagrams, Design Rules and Layout • Lambda(λ)-based design rules for wires, contacts and Transistors • Layout Diagrams for NMOS and CMOS Inverters and Gates • SPICE Modelling, SPICE Tutorials and Commands • Sources and Passive Components	**20**
OUTCOME-8: Students will able to understand various Design verification techniques like UVM, OVM and AVM.	• Introduction UVM, UVM Object	**20**
	Grand Total	**200**

***Assessment for the Qualification will be conducted as per the guidelines as applicable from time to time.**

SECTION 2

25. EVIDENCE OF LEVEL

Title/Name of qualification/component: Post Diploma in VLSI Design, Tools and Technology. Level:5			
NSQF Domain	**Outcomes of the Qualification/Component**	**How the outcome relates to the NSQF level descriptors**	**NSQF Level**
Process Required	After going through this module student		**5**

	will Understand the basics of VLSI, Hardware- Software tools They can Explore the Basics of Verilog. They will gain basic knowledge the of system designing in VLSI.	Students are introduced to the knowledge of the subject, and comprehension is strengthened with interactive Q&A and short quizzes. They will be able to explain and generalize knowledge in VLSI. Students acquire hands-on experience in using CAD tools in VLSI design, and apply what they have learnt in lectures/tutorials to do a mini-project on the design of a sub-system.	
Professional Knowledge	Student would be able to design different Analog and digital system by synthesis, place, and routing.	To be able to understand designed functional Analog and digital system To perform synthesis, place, and route of a Mixed signal design into a target FPGA. To display knowledge of good digital design practices in the context of the target hardware. To learn advanced VLSI design using EDA Tools	**5**
Professional Skill	Students would be able to know how to work with EDTA tool for development of VLSI systems using different Hardware and Software	Handling of EDA tools Hardware and Software for development of VLSI Circuitry. Handling of prototype and pre-production VLSI product for various electronic system and liaise with supplier	**5**

		Able to specify components and equipment required for product development.	
Core Skill	Can coordinate with different VLSI companies to design different electronics systems and circuits.	Providing support for VLSI Design Group Able to give support and advice whenever necessary to all stakeholders involved. Over the whole product life cycle, ensure that the products meet the quality standards	**5**
Responsibility	Responsible for designing different VLSI systems using latest technologies	The candidate will learn various aspects of VLSI design	**5**

Means of Assessment:

T1 (TP1): Theory paper 1
T2 (TP2): Theory paper 2
P(P): Practical paper comprising 2 practical exams (P-1, P-2) 1 for each module.
IA: Internal Assessment
AS & P: Project

Examination Pattern:

Sl No	Examination Pattern	Modules Covered	Duration in Minutes	Maximum Marks
1	Theory Paper – 1: Fundamentals of System and Information Security	Module 1 & 2	90	100
2	Theory Paper – 2: Advanced Computer Concepts	Module 3, 4, 5	90	100
3	Practical -1	Module 1 to 5	180	90
4	Internal Assessment	Module 1 to 5	-	30
5	Project/Presentation /Assignment	Module 1 to 5	-	30
	Total			**350**

SECTION 3

EVIDENCE OF NEED

26	**What evidence is there that the qualification is needed? What is the estimated uptake of this qualification and what is the basis of this estimate?** **Need of the Qualification and industry relevance** VLSI (Very Large Scale Integration) has emerged as a very significant technology to provide tremendous quantum of process technologies for MEMS, NEMS and RF components, many of the formerly external components can now be integrated into a single System-on-Chip which has resulted in a dramatic improvements in performance while achieving reduction in the size, cost and power consumption Complexity in such systems arises not only from the diversity of the technologies, from sensors and actuators and RF front-ends to base-band DSP software, etc., that must be integrated on-chip comprising of tens of millions of transistors, but also from the fact that such systems must be increasingly built from parts that have been designed separately and using different tools and flows. **Estimated uptake:** 10 students / Batch and 4 Batches / Year
27	**Recommendation from the concerned Line Ministry of the Government/Regulatory Body. To be supported by documentary evidences** NA
28	**What steps were taken to ensure that the qualification(s) does/do not duplicate already existing or planned qualifications in the NSQF?** It has been checked in National Qualification Register for similar courses.
29	**What arrangements are in place to monitor and review the qualification(s)? What data will be used and at what point will the qualification(s) be revised or updated?** The Qualification is to be monitored and reviewed every three years. The following data will be used ● Results of assessments ● Employer feedback regarding student skill after conducting a placement drive ● Employer feedback will be sought post-placement ● Student feedbacks ● Workshops and seminar for reviewing the qualifications

	• Consultation/ Tie-up with self-help groups, Industries, Expert for review of the Curriculum so as to meet the changing pace of technology and general health care requirements.

SECTION 4
EVIDENCE OF PROGRESSION

30	**What steps have been taken in the design of this or other qualifications to ensure that there is a clear path to other qualifications in this sector?** This QF is a specialised tool training and there is no higher level qualification found available in the NQR at present