QUALIFICATION FILE

Revised Application Documentation: Version 1 /10 October, 2016

NSDA Reference
To be added by NSDA

CONTACT DETAILS OF SUBMITTING BODY

Name and address of submitting body:

Centre for Development of Computing, Advanced Computing Training School (CDAC, ACTS)

Innovation Park, Punchwati, Pashan Road

Pune

Name and contact details of individual dealing with the submission

Name: Shri. Aditya Kumar Sinha

Position in the organisation: Principal Technical Officer

Address if different from above

Tel number(s): 020-25503155

E-mail address: saditya@cdac.in

List of documents submitted in support of the Qualifications File

There are opportunities to submit supporting documents throughout the Qualification File template. The titles of all these documents should be listed here.

1. Course Content
2. Industry Feedback
3. Alumni Feedback

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SUMMARY

Qualification Title and Code:	PG-Diploma in VLSI Design
Body/bodies which will award the qualification:	Centre for Development of Advanced Computing (C-DAC) organization of the Ministry of Electronics and Information Technology, Govt. Of India
Body which will accredit providers to offer the qualification:	CDAC
Body/bodies which will be responsible for assessment:	CDAC
Occupation(s) to which the qualification gives access:	PG-DVLSI is a pioneering course offered by C-DAC to assist engineers who wish to gain theoretical as well as practical knowledge in the field of Very Large Scale Integration (VLSI) design. It will also prepare them to keep pace with the changing trends of VLSI technology and the requirements of an ever-growing VLSI design industry. The entire course syllabus, courseware, teaching methodology and the course delivery have been derived from the rich research and development background of C-DAC, which has a legacy of designing the PARAM range of supercomputers. At the end of the course students will be able to do field-programmable gate array (FPGA) implementations, application-specific integrated circuit (ASIC) designs, CMOS design and SoCs in VLSI industry as VLSI designer/ chip designer and verification engineer. Students will also be able to develop a programmable chip using verilog and system verilog languages.
Proposed level of the qualification in the NSQF:	Level 8
Anticipated volume of training/learning required to complete the qualification:	900 hrs of classroom/lab learning (6 Months full time course)
Entry requirements / recommendations:	1. Graduate in Engineering or equivalent (e.g. BE / BTech / 4-year BSc / AMIE / DoEACC B Level, etc.) in Electronics/ Computer Science/ IT or related areas, 2. OR Post Graduate in Engineering Sciences (e.g. MSc in Computer Science, IT, Electronics, etc.) 3. The candidates must have secured a minimum of 55% marks in their qualifying examination.

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Progression from the qualification:	These candidates will be trained in various VLSI Technologies, Project implementations and Management skills. They can start career as VLSI designer/ chip designer, verification engineer/tester and leads to project lead/manager or Entrepreneur after having relevant experience. Candidate can start from level 8 and lead to further levels.
Planned arrangements for RPL:	NA
• International comparability where known:	• Course which covers field- programmable gate array (FPGA) implementations, application-specific integrated circuit (ASIC) designs, CMOS design and SoCs and verilog and system verilog languages in six months full time courses are not available. Various institutes are running courses but as sub set of this courses like: • Maven Silicon Bangalore is running various VLSI courses (http://www.maven-silicon.com/) • Harvard University (https://www.extension.harvard.edu/academics/courses/course-catalog) • NIU (National Ilan University) Taiwan http://ecewww.niu.edu.tw/zh_tw/Introduction/DeptIntroduction

Formal structure of the qualification:

Title of NOS/unit or other component (include any identification code used)	**Mandatory/ Optional** Enter M or O for each unit/ component	**Estimated size (learning hours)** The total should be the same as the entry under "anticipated volume" above	**Level** In the NSQF, individual units or components of qualifications can have outcomes which put them at levels which are higher or lower than the whole qualification.
Advanced Digital Design	M	24	8
System Architecture	M	36	8
Programming Fundamentals	M	70	8
High Level Design Methodology	M	110	8

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HDL Simulation and Synthesis	M	110	8
Verilog	M	120	8
ASIC Design Issues	M	40	8
CMOS VLSI Design	M	20	8
Verification using System Verilog	M	90	8
Linux shell scripting & Perl	M	60	8
Effective Communication	M	50	8
Aptitude & English	M	50	8
Project	M	120	8

Please attach any document giving further detail about the structure of the qualification – eg a Curriculum or Qualification Pack.
Give details of the document here:

SECTION 1

ASSESSMENT

Body/Bodies which will carry out assessment:
CDAC's Exam, Evaluation and Certification department will carry out assessment as per evaluation guideline finalized by Academic Council/ Academic Management Committee.

Will the assessment body be responsible for RPL assessment?

- Same will be finalised when the national RPL Policy will be finalised.
- Assessment is online through our CCAT system.
- Issuance of qualification is centralized through CDAC.

Describe the overall assessment strategy and specific arrangements which have been put in place to ensure that assessment is always valid, consistent and fair and show that these are in line with the requirements of the NSQF:

Assessment is a necessary and essential part of conducting the Post Graduate Diploma in VLSI Design, as it provides important feedback and inputs to both the institute as well as the student. The institute gets an idea about the relative performance of each student, which also serves as feedback about the design and conduct of the course. The student gets a clear picture of his academic standing, individually and in comparison to his fellow students.

- A separate evaluation process is to be conducted for every module of the course.
- The evaluation for each module must be completed as per guidelines given below. The mid-module /surprise test evaluation is mandatory and can be taken after discussion with the concerned faculty.
- Students are evaluated on a continuous and throughout the duration of the course to make a fair assessment of the skills acquired by them. To have a very uniform and fair assessment.

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The evaluation process is divided into two parts:

- Continuous Assessment - CA (60 marks)
- Course End Examination - CCE (40 marks)

Continuous Assessment: This is being done primarily by the respective faculty in the form of Lab tests, assignments, quizzes etc conducted (with the help of the respective course co-coordinators) at regular intervals and as and when the portions of the modules are completed. These are basically internal exams and local to the centre. This process is further categorized into two parts.

- Lab test (40 marks)
- Internal test (20 mark): Assignment/Case Studies /quiz and other valuation methods like case study, viva, group discussion depending on the subject and the faculty (20 marks)

It is recommended to conduct the Effective Communications & Aptitude sessions for the benefit of the students and also conduct some surprise test for Effective Communications & Aptitude sessions.

The figures shown below indicate the weightage of each module in the final performance statement. The examination(s) for each module must be conducted for at least that number of marks. However, the centre may conduct evaluation for a higher number of marks, in which case the marks will be scaled down. For example, if the examination for the Advanced Digital Design module is conducted for 100 marks, the marks earned by the student will be scaled down to out of 40.

A student must score a minimum of 40 percent marks in each component of the evaluation, and also in the aggregate score, in order to successfully clear the module. If a student scores more than 40% on aggregate but has scored less than 40% in one component of the evaluation, he will not be declared as passed.

The weight age for each component will normally be:

Theory examination – (CCEE)	40%
Laboratory examination	40%
Internal marks	20%

(Internal marks: Lab Assignment Evaluation, Surprise Tests, attendance, Viva, Seminars)

The question papers for the theory as well as the laboratory examinations at all the centres will be set by CDAC, ACTS Pune. The centres according to guidelines provided by C-DAC, ACTS Pune, will conduct the evaluation of the laboratory and assignments locally.

Minimum Pass marks:

The minimum marks to be obtained for declaring a student pass in any module is as follows:

For 40 mark QP	:	16 marks
For 20 mark QP	:	8 marks
For 60 mark QP	:	24 marks

Assessment is through CCAT system.

About CCAT System:

An Image based, LAN based, secure, fault tolerant and scalable system through which examinations can be delivered "on demand" basis in selected examination centres spread across the country.

System Support:

- Decentralized mode of operation(LAN based)

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- Question Paper approach
- Multi lingual and multi subject support
- Browser based

Components of the CCAT System Includes:

- **Registration System**- To register the candidate for examination.
- **Authoring Tool** -To generate an image based encrypted question paper.
- **Examination System** -To manage the examination related activity and conduct- i.e Registration data and question paper uploading, conduct of examination, response generation
- **Result Processing System** -To generate the result for the particular examination and paper.

Salient Features:

- Provides end to end security as Question paper is encrypted and decrypted just minutes prior to the examination.
- Highly Scalable and support up-to 1000 candidate per center per session.
- Highly fail safe with ability to resume exam on the last saved state.
- Isolated examination Network unconnected to any other network including Internet.
- Simple and user friendly interface for Candidate
- Minimal Requirements on the client machine (just a compatible browser).
- Minimum Server requirement at each exam centre (2 Laptops -> one for redundancy).
- Question paper independent of languages, font and symbols
- Resilient to server failures
- Identical URL for Mock test and Actual exam
- Provides end-to-end audit log

Feedback System: C-DAC's Advanced Computing Training School (ACTS) offers various courses and training programs through its own training centres and its network of Affiliated Training Centres (ATC) spread across the country. Each year, thousands of students and professionals are trained at these centres.

The purpose of the system i.e. Online Feedback System (OFS) is to develop a web application for getting the online faculty feedback by the students studying at C-DAC centers and also at the various Authorized Training Centres (ATC) affiliated to C-DAC for different training programs offered by CDAC ACTS.

This system is for conducting "The Student Survey" for quality assurance of education. Students, Faculties and administrators can all benefit from survey. This is helpful in the continual improvements in teaching programs, processes as well as infrastructure and thereby enhancing the students' learning experience at CDAC ACTS.

The Online Feedback System make the student feedback procedure centralized for all CDAC centres

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as well as various Authorized Training Centres (ATCs) located across the country through which headquarter manager can manage student feedback of faculties as well as infrastructure studying at different C-DAC training centres with different reports for feedback analysis.

Please attach any documents giving further information about assessment and/or RPL.
Give details of the document(s) here:

ASSESSMENT EVIDENCE

Each module should be evaluated as per the weightage given below.

Sr. No.	Module	Learning Outcome	Theory	Lab	IA	Total Marks
1	Advanced Digital Design	• Good understandability of Digital electronics that helps in circuit designing • Knowledge of State Machine to design circuits • Better understanding of design issues like metastability, noise margins, power, fan-out, design rules, skew, timing considerations.	40	-	60	100
2	System Architecture	• Basic of Computer Architecture (ARM and FPGA) • Demonstrate understanding of USB and PCI • Knowledge of Memory Architectures (RAM, ROM, Cache)	40	-	60	100
3	CMOS VLSI Design and ASIC Design	• Basic of Backend designs using CMOS • Demonstrate				100

		understanding of different design issues like Antenna effect, Electro migration effect, Body effect, Inductive and capacitive cross talk and Drain punch through, etc. • Design of complex circuit fabrication steps of IC`s • Demonstrate understanding of Fault detection techniques BIST	40	40	20	
4	VHDL, HDL Simulation and Synthesis	• Master in the basic elements of VHDL programming: variables, flow control and functions/task • Good knowledge of Concurrent & Sequential statements • Demonstrate understanding of Test Bench and Simulation using VHDL • Experts in VHDL using Synthesis tools (Xilinx) • Capable to design a chip using VHDL	40	40	20	100
5	Verilog (In accordance with IEEE 1364-2005 and 2009)	• Master the basic elements of Verilog programming: variables, flow control and functions/task • Good knowledge of Test Bench and Simulation using Verilog • Experts in Verilog	40	40	20	100

		using Synthesis tools (Xilinx) • Capable to design a chip using Verilog				
6	Programming fundaments, Linux Shell Scripting & Perl	• Master the basic elements of imperative programming: variables, flow control and functions • Effectively use industry standard tools for writing, testing, and running C++ code • To convert mathematical statements, such as functions, into C++ code. • Choose and apply the required Linux commands to develop C++ programs in a command-line environment. • Good understanding of Linux Shell Programming • Effectively use industry standard tools for writing, testing, and running perl scripts	40	40	20	100
7	Verification using System Verilog	• Capable to verify circuits and modules using System Verilog • Students can able to create testing and verification environment • Master in basic elements of System Verilog programming: variables flow	40	40	20	100

		control, interface, programming Blocks and functions. • Basic of UVM Verification Methodology				
8	Aptitude and Effective Communication	Students will be able to: • apply general mathematical models to solve a variety of problems • solve problems and correctly arrive at meaningful conclusions regarding their answers • manipulate equations and formulas in order to solve for the desired variable • interpret given information correctly, determine which mathematical model best describes the data, and apply the model correctly • Use theories of interpersonal communication to explain and evaluate their own behavior in interpersonal relationships. • Synthesize and apply appropriate and effective conflict management strategies.				**Grade**
9	Project	• Design, implement and evaluate				**Grade**

		computer technologies, systems, processes, components and/or programs appropriate to a defined task, while analyzing the impact on existing systems and potential future applications. • Think critically, creatively and analytically in developing technological solutions to simple and complex problems. • Apply formal frameworks, methods and management systems to the organization, storage and retrieval of data in ways that demonstrate an understanding of both the business enterprise and the relevant technology. • Implement effective business solutions across an organization that demonstrates appropriate consideration of alternative computer technologies, including networks, servers,				

		programming languages and database systems. • Plan, analyze, design and construct information systems to identified specifications, using clear and efficient code in the relevant programming language(s). • Work effectively in a team to analyze the requirements of a complex software system, and solve problems by creating appropriate designs that satisfies these requirements • communicate to others the progress of the system development and the content of the design by means of reports and presentations				

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Complete a grid for each grouping of NOS, assessment unit or other component as listed in the entry on the structure of the qualification on page 1.

Title of NOS/Unit/Component:

Assessable outcomes	Assessment criteria for the outcome
Enter the learning outcomes /elements of competence which will be assessed.	List all the criteria applying to this element/outcome.
All the modules of PG-DVLSI	**A+ >= 85%,** **A >= 70% to < 85%** **B >= 60% to < 70 %** **C >= 50% to < 60%** **D >= 40% to < 50%** **F < 40%**

Means of assessment 1

Theory portion Assessment will be done through LAN based online system. Paper will be Objective question based. Lab exam will be done separately as per evaluation Guidelines.

Means of assessment 2

Re-examinations:

The following conditions will be applicable for the course end re-exam:

- Students who do not appear for an exam on the scheduled date will not have an automatic right to re-examination. Only those students who, in the opinion of the centre/course coordinator have a genuine reason for being absent may be allowed to appear for a re-exam.
- Students who have failed an exam may be allowed to appear for a re-exam.
- The re-exam should be conducted following the same process as the regular examination.
- Students, who failed/remained absent in the Course End Examination conducted by C-DAC, shall be allowed to appear in the re-examination only once.
- Students who remain absent or fail in the re-examination will not get any further chance for appearing for the re-examination. In such case the candidate can receive the Performance Statement and the certificate of participation without any grade.
- On evaluation of their answer sheets 20% of the marks obtained by the students will be deducted (towards de-rating for re-examination) for arriving at the final score, i.e. in order to clear the module test the student has to score a minimum of 48% marks instead of 40%.
- There will be no re-exam for the re-exam

Pass/Fail:

If Candidate scored below 40% in any of the component like Theory, lab or Internal will be consider as FAIL.

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SECTION 2

SUMMARY EVIDENCE OF LEVEL

Level	Process Required	Professional Knowledge	Professional Skill	Core Skill	Responsibility
8	**Comprehensive, cognitive, theoretical knowledge and practical skills to develop creative solutions to abstract problems. Undertakes self-study; demonstrates intellectual independence, analytical rigour and good communication**			**Exercise management and supervision in the context of work/study having unpredictable changes; responsible for the work of others.**	

Assessed outcome	Process Required	Professional Knowledge	Professional Skill	Core Skill	Responsibility
1. Advanced Digital Design	Candidate has knowledge of Programming language, HDL Simulation and Synthesis, verilog, Verification using System Verilog, Linux shell scripting & Perl and communication skills. So candidates can develop creative solution to abstract problems. Undertakes self-study; demonstrates intellectual independence, analytical rigour and good communication.			Candidate will be learning effective communications. Language to communicate written and oral. Aptitude, basic understanding of social political and natural environment. Candidate has knowledge of Management project and supervise the activity plan in the context of work/study having unpredictable changes; responsible for the work of others.	
2. System Architecture					
3. Programming Fundamentals					
4. High Level Design Methodology					
5. HDL Simulation and Synthesis					
6. Verilog					
7. ASIC Design Issues					
8. CMOS VLSI Design					
9. Verification using System Verilog					
10. Linux shell scripting & Perl					
11. Effective Communication					
12. Aptitude & English					
13. Project					

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SECTION 3

EVIDENCE OF NEED

What evidence is there that the qualification is needed?

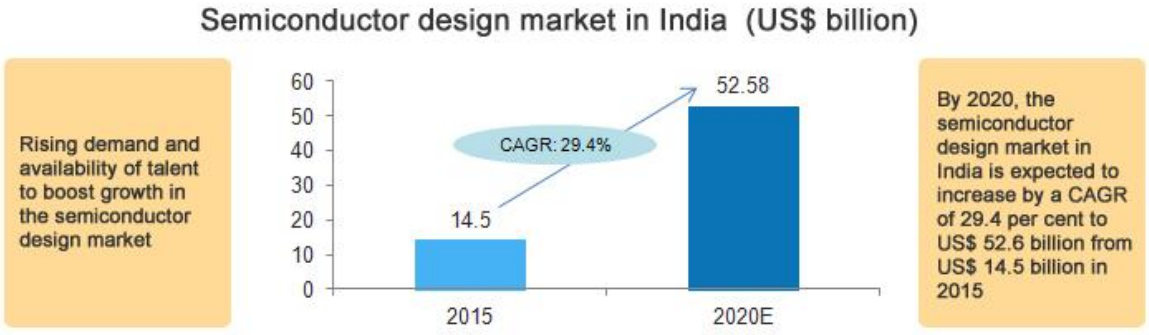
C-DAC set up the Advanced Computing Training School (ACTS) in 1993 to meet the ever-increasing skilled manpower requirements of the Information Communication Technologies (ICT) industry as well as supplement its intellectual resource base for cutting-edge research and development. Over the years C-DAC has designed and delivered various postgraduate and undergraduate degree and diploma programmes. In addition, C-DAC imparts ICT training to state and national governments and agencies, strategic sectors, corporate and industries, foreign countries and international students, based on specific requirements.

PG-DVLSI is our one of advanced course in VLSI domain and has not been contested till date.

The Education and Training activities of C-DAC are governed and steered by Academic Council (AC) and Academic Management Committee (AMC). As per the Academic Council minutes and direction, a syllabus updation subcommittee is formed by combining members from different C-DAC centers. The sub-committee gave their inputs for syllabus updation. The resource centre has conducted meetings for updating required modifications in the current syllabus of PG-Diploma. After minutes of the meeting with draft syllabus contents were circulated across all the participating centers for any suggestion and comments. If any suggestions come through discussion of all concerned members, we incorporate the same and circulate again for finalization. After that we make the source book and informed to all centers for their review

What is the estimated uptake of this qualification and what is the basis of this estimate?

Total uptake of course is 160 per batch. India has a very fast growing electronics system design manufacturing (ESDM) industry. India also has a strong design base with more than 120 units. According to the Department of Electronics and Information Technology (DeitY), nearly 2,000 chips are being designed every year in India and more than 20,000 engineers are working on various aspects of chip design and verification. As per the reports Department of Electronics & Information technology to grow to US $ 52.6 billion by 2020 Indian Share is US$ 14.5 billion by 2015.



Source: Department of Electronics & Information Technology; Indian Semiconductor Association; E-Estimated; CAGR - Compounded Annual Growth rate

Link: http://www.ibef.org/industry/semiconductors.aspx

What steps were taken to ensure that the qualification(s) does/do not duplicate already existing or planned qualifications in the NSQF?
NA

What arrangements are in place to monitor and review the qualification(s)? What data will be used and at what point will the qualification(s) be revised or updated?

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manpower requirements of the Information Communication Technologies (ICT) industry as well as supplement its intellectual resource base for cutting-edge research and development. Over the years C-DAC has designed and delivered various postgraduate and undergraduate degree and diploma programmes. In addition, C-DAC imparts ICT training to state and national governments and agencies, strategic sectors, corporate and industries, foreign countries and international students, based on specific requirements.

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SECTION 4

EVIDENCE OF RECOGNITION AND PROGRESSION

What steps have been taken in the design of this or other qualifications to ensure that there is a clear path to other qualifications in this sector?

- This qualification has been designed in consultation with industry and domain expert keeping in mind today's need. Evaluation criteria have been added to ensure progression to related path ways identified as per career path.
  Below are some feedback :
  https://www.quora.com/What-are-the-job-prospects-of-PGDVLSI-at-CDAC/answer/Shruti-Gupta-226

- Alumni feedback attached as annexure.

Please attach any documents giving further information about any of the topics above.
Give details of the document(s) here:

1. Course Content (Annexure –I)
2. Feedback from Alumni (Annexure –II)
3. Industry Feedback (Annexure –III)
4. Feedback from Training centres (Annexure –IV)
5. Placement Statistics(Annexure-V)